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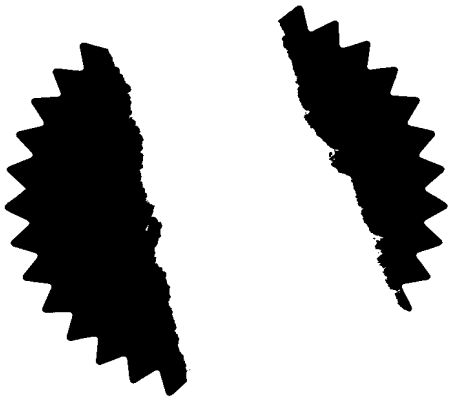

Signed K Behen

Dated 4 August 2003

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Patents (1977)
(Rule 16)

THE PATENT OFFICE
A
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1/77
OCT02 E752224-1 002319
1/77D 0.00-0222691.8

Request for grant of a patent

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The Patent Office

Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference — SC0969EI/DJM/GBRI/JB/WEIZMAN

2. Patent application number *(The Patent Office will fill in this part)* — 0222691.8 — 1 OCT 2002

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

MOTOROLA, INC
1303 EAST ALGONQUIN ROAD,
SCHAUMBURG, ILLINOIS 60196,
U.S.A.

Patents ADP number *(if you know it)* 08281107001 — 5001976903

If the applicant is a corporate body, give the country/state of its incorporation — U.S.A. — DELAWARE

4. Title of the invention — ANALYSIS MODULE, INTEGRATED CIRCUIT, SYSTEM AND METHODE FOR TESTING AN INTEGRATED CIRCUIT

5. Name of your agent *(if you have one)*

MCCORMACK DEREK J
EUROPEAN INTELLECTUAL PROPERTY DEPARTMENT
MIDPOINT
ALENCON LINK
BASINGSTOKE
HAMPSHIRE RG21 7PL
UK
ADP NO. 00001180006

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

Patents ADP number *(if you know it)*

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

☒ YES ☐ NO

Patents Form 1/77

9. For the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	15
Claim(s)	4
Abstract	1
Drawing(s)	11 + 11

CF

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	4
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	1
Any other documents *(please specify)*	1 x FEE SHEET

11. I/We request the grant of a patent on the basis of this application.

Signature DJMcCormack Date 30/9/02

12. Name and daytime telephone number of person to contact in the United Kingdom

MCCORMACK DEREK J

Julia BRAMHALL 01256 790002

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

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Patents Form 7/77

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(Rule [illegible])

The Patent Office

7/77

Statement of inventorship and of right to grant of a patent

The Patent Office

Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference **SC0969EI/DJM/GBRI/JB/WEIZMAN**

2. Patent application number *(if you know it)* 0222691.8

3. Full name of the or of each applicant **MOTOROLA, INC**
1303 EAST ALGONQUIN ROAD,
SCHAUMBURG, ILLINOIS 60196,
U.S.A.

4. Title of the invention **ANALYSIS MODULE, INTEGRATED CIRCUIT, SYSTEM AND METHODE FOR TESTING AN INTEGRATED CIRCUIT**

5. State how the applicant(s) derived the right from the inventor(s) to be granted a patent
THE APPLICANT IS ENTITLED TO THE INVENTION BY VIRTUE OF THE INVENTORS EMPLOYMENT

6. How many, if any, additional Patents Forms 7/77 are attached to this form?
(see note (c))

7. I/We believe that the person(s) named over the page *(and on any extra copies of this form)* is/are the inventor(s) of the invention which the above patent application relates to.

Signature D J McCormack Date

MCCORMACK DEREK J **30/9/02**

8. Name and daytime telephone number of person to contact in the United Kingdom **Julia BRAMHALL** **01256 790002**

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a) If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

WEIZMAN, YOAV

MOTOROLA SEMICONDUCTOR
HERZELIA
1 SHENKAR ST. INDUSTRIAL ZONE
46120 HERZELIA
ISRAEL

Patents ADP number *(if you know it)*: 8474553001

SHPERBER, SHAI

MOTOROLA SEMICONDUCTOR
HERZELIA
1 SHENKAR ST. INDUSTRIAL ZONE
46120 HERZELIA
ISRAEL

Patents ADP number *(if you know it)*: 8474561001

BARUCH, EZRA

MOTOROLA SEMICONDUCTOR
HERZELIA
1 SHENKAR ST. INDUSTRIAL ZONE
46120 HERZELIA
ISRAEL

Patents ADP number *(if you know it)*: 8474575001

Reminder

Have you signed the form?

ANALYSIS MODULE, INTEGRATED CIRCUIT, SYSTEM AND METHOD FOR TESTING AN INTEGRATED CIRCUIT

Field of the Invention

This invention relates to testing and failure analysis of Very Large Semiconductor Integrated circuit (VLSI) devices and particularly but not exclusively to testing of devices using failure analysis tools.

Background of the Invention

The testing and failure analysis of integrated semiconductor devices is well known and a number of Failure Analysis (FA) tools have been developed. For example it is known from US patent number 5,760,892 to provide a method of analyzing failure of a semiconductor device using an emission microscope.

It is also known from US patent no. 6,153,891 to provide a method and apparatus providing a circuit edit structure through the backside of an integrated circuit die.

It is also known from US5294812 to provide a semiconductor device having an identification region which may be inspected by eye in order to discern information about the device.

Typically, such FA tools are used to measure and evaluate the performance of an integrated circuit are specified by physical signal parameters such as rise time, timing/jitter measurements, spatial visible resolution between diffusion/metals and crosstalk between adjacent phase-shifted signals. These parameters are measured and used to define performance criteria for the integrated circuit.

A known problem with such arrangements is that the abovementioned physical parameters are not readily isolated and identified from within the integrated circuitry. Particularly in the field of new and emerging process technologies and materials, calculations and derivations of the performance criteria must be made during the analysis itself, often in an iterative way, leading to a lengthy and complex procedure.

A need therefore exists for an analysis module, integrated circuit, system and method for testing an integrated circuit wherein the abovementioned disadvantage(s) may be alleviated.

Statement of Invention

In accordance with a first aspect of the present invention there is provided an analysis module as claimed in claim 1.

In accordance with a second aspect of the present invention there is provided an integrated circuit as claimed in claim 2.

In accordance with a third aspect of the present invention there is provided a system as claimed in claim 3.

Preferably the submodule test structure is chosen in dependence upon the analysis tool(s) to be used in subsequent testing.

In accordance with a fourth aspect of the present invention there is provided method for testing integrated circuit functionality as claimed in claim 5.

Preferably the submodule test structure(s) includes a calibration structure and/or a probing structure and/or optical alignment means.

The submodule test structure is preferably isolated from the function modules. Preferably the testing includes failure analysis.

In this way an analysis module, integrated circuit, system and method for testing an integrated circuit is provided in which rapid and inexpensive testing and failure analysis of an integrated circuit are facilitated.

Brief Description of the Drawings

One analysis module, integrated circuit, system and method for testing an integrated circuit incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1 shows a system for testing an integrated circuit in accordance with the invention;

FIGS. 2, 5, 7, 8, 12, 13 and 14 show block schematic diagrams of different submodule test structures in accordance with different aspects of the present invention;

FIGS. 3 and 4 show topological diagrams of the test structures of FIG. 2;

FIG. 6 shows a topological diagram of the structure of FIG. 5;

FIGS. 9, 10 and 11 show topological diagrams of the test structures of FIG. 8; and

FIG. 15 shows an illustrative flow diagram of a process of fabricating and testing an IC in accordance with the present invention.

Description of Preferred Embodiment(s)

Failure Analysis (FA) instruments used for analysis of an Integrated Circuit (IC) die typically operate by taking measurements relating to the circuitry through the backside of the die. These measurements are then used to Locate the failure by measuring various physical aspects or parameters of the IC.

Referring to FIG. 1, there is a system 5 shown for testing an Integrated Circuit (IC) 10 according to the present invention. The system incorporates a number of FA instruments: as a laser voltage probing system 40, a Time Resolved Emission Microscope (TRLEM) 50 and an Infrared Emission Microscope (IREM) 60. The system also incorporates electrical characterization equipment 70.

The IC 10 includes a first semiconductor area comprising function modules 20 and a second semiconductor area comprising an analysis module 30. The analysis module 30 includes four submodules 32, 34 36 and 38 respectively, to be further described below. The function modules 20 are those elements of the IC 10 which perform the normal operating functions of the IC 10.

As relatively little semiconductor material is required to implement the analysis module 30, areas of semiconductor material on the die not used for the operation modules 20 are utilised for the analysis module 30 and a change in die size is therefore not required in order to implement the present invention. It will be

appreciated that the submodule test structures of the analysis module 30 need not occupy contiguous space on the integrated circuit 5.

The design of sub-modules 32, 34, 36 and 38 of the analysis module 30 are chosen according to the FA instruments 40, 50 and 60 and the electrical characterization equipment 70 to be used. In this way the appropriate test structures for the FA instruments 40, 50 and 60 respectively and for the electrical characterization equipment 70 are provided by the sub-modules 32, 34, 36 and 38 respectively, and the system performance evaluation and calibration may be readily performed in a manner to be further described below.

The laser voltage probing system 40 shown in FIG. 1 exploits InfraRed (IR) laser based techniques to allow signal waveforms and high frequency timing measurements to be derived directly from P-N junctions of a semiconductor structure through the silicon backside substrate in a flip-chip mounted IC packages.

Referring now also to FIG. 2 there is shown a block schematic diagram of a circuit 100 having physical structures depicted in FIG. 3 and FIG. 4. The circuit 100 has a number of submodule structures to be used in conjunction with the laser system 40 in order to derive the following performance evaluation criteria:

a) Spatial visible resolution between two adjacent diffusions:

Referring now also to FIG. 3, which shows the physical topology of the circuit 100 of FIG. 2, diffusions are provided at various distances starting from a minimum distance 110 of approximately 0.18um to a maximum distance 120 of 0.72um.

b) Cross talk between adjacent phase shifted signals:
Referring now also to FIG. 4, which shows the physical topology of the circuit 100 of FIG. 2, a leading diffusion 130 is surrounded with 4 diffusions 140 that carry a retarded signal. This structure is duplicated several times with different distances between the active areas, as shown by structures 150, 160 and 170 respectively.

Referring now also to FIG. 5 there is shown an inverter chain circuit 200 used to generate the phase shifted signal. Alternatively the phase shifted signal may be provided by using different clock input. Cross talk may be measured in different frequencies and also with an asynchronous signal to create noise.

c) Sensitivity - Minimum measurable gate/diode area and voltages:
The diffusions shown in FIG. 3 provide structures of varying geometry and area.

d) Diodes Vs transistors:
Referring now also to FIG. 6, which shows the physical topology of the circuit 200 of FIG. 5, signals are sampled from diodes and from the inverters in the chain.

FIG. 6 depicts structures having transistors of various gate area and loads.

e) P Vs N diodes:
The diode structure is duplicated as P type for comparison.

The TRLEM (Time Resolved Emission Microscope) 50 shown in FIG. 1 uses sensitive IR detector to acquire faint signals of switching transistors, to provide precise identification of defect location.

Normally biased CMOS logic circuits emit photons only in a short period during switching transients, allowing precise timing of individual transistors.
The emitted light can be detected from the front or back side of an IC die. A high sensitivity detector can determine the exact timing of the photon emission. A detector array can also determine the location.

Referring now also to FIG. 8 there are shown a number of submodule structures to be used in conjunction with the TRLEM 50 in order to derive the following performance evaluation criteria:

a) Sensitivity - Minimum measurable gate area load and voltages:
Referring now also to FIG. 6, eight transistors of various gate area and loads are shown (transistors 210-280).

b) Spatial visible Resolution between two adjacent transistors:
Transistors are provided at various distances starting from a minimum distance of approximately 0.18um to a maximum distance of approximately 1.44um. (Transistors 210, 220, 230 and 240 of FIG. 6)

c) Cross talk between adjacent transistors carrying phase shifted signals:
leading inverter will be enveloped with 4 inverters that carry retarded signal. (Transistors 210, 220, 230 and 240 of FIG. 6) This structure will be present with four different distances between the active area and inverter sizes. (Transistors 250, 260, 270 and 280 of FIG. 6). The retarding signal will be generated from the inverter chain circuit 200 itself.

d) Load impact:
Load is especially influential on TRLEM measurements. Various inverters with various load capacitance will allow parametric analysis of load impact, as shown in FIG. 7.

e) P vs. N emissions:
These signals will be sampled (if resolution permits) from complementary transistors.

f) Measurements on NAND and NOR structures.

The IREM 60 shown in FIG. 1 utilises a cryogenically cooled HgCdTe (MCT) imaging focal plane array that have

spectral response of 0.8-2.5 um. Several experiments show that photo-emission from a transistor in various emission states(forward bias, saturation, latch-up or gate oxide breakdown) extend beyond the 1.1 um into the near-IR. The IREM 60 is capable of detecting these emissions.

Referring now also to FIG. 8, there are shown a number of submodule structures to be used in conjunction with the IREM 60 in order to derive the following performance evaluation criteria:

a) Sensitivity, the minimum measurable emission Vs gate area:
Referring now also to FIG. 9, transistors of various gate width are provided, in order that a minimum detectable emission area may be evaluated.

b) Resolving power between two adjacent emission spots: a set of identical transistors are placed at incremental distances.

c) Geometry and other physical parameters relation to emission:
Referring now also to FIG. 10, transistors with various width and lengths are provided.

d)Current and voltage dependence:
the gate and source of each transistor may be controlled independently of the gate level, as shown in FIG. 8.

e) Substrate current - substrate will be connected to separate supplies, as shown in FIG. 8.

Referring now also to FIG. 11 there is shown a series of test structures forming an imaging block. The purpose of these structures is to evaluate the imaging capabilities for the different layers, from the backside, of the different FA tools. The imaging capabilities will be examined in x- and y-axes with lines spaced at various distances. It is also possible to examine the best fiducial characteristics for Computer Aided Design (CAD) navigation alignment with the various tools.

The submodule 38 of FIG.1 is used in conjunction with the electrical characterization equipment 70 in order to characterize the AC parameters of the process.

As performance increases, and the performance margin of devices becomes critical, the electrical structures for AC characterization of process parameters serve as an indication and calibration point for other functional speed paths in the device. Comparison between the circuit simulation and the electrical structures performance provide the means to simulate functional speed paths with greater accuracy, and to investigate the degradation in AC performance of a device.

The structures for electrical characterization may include single components such as inverter, a latch, a Flip-Flop, or a Random Access Memory (RAM) bit cell. They may also include dedicated circuits such as a Ring

oscillator or a part of functional speed path. Referring now to FIG. 12 there is shown a single latch. Referring now to FIG. 13 there is shown a ring oscillator comprising a number of latches as depicted in FIG. 12. Referring now to FIG. 14 there is shown a ring oscillator comprising a number of inverters.

Referring now also to FIG. 15 there is shown an illustrative flow diagram of a process of fabricating and testing an IC such as the IC 10 of FIG. 1 in accordance with the present invention.

The process starts at block 700, and the first step (block 710) is to select the FA tool or tools which will be used to perform the testing and failure analysis. Then the submodule test structures appropriate for the selected FA tool(s) are selected (block 720). This may be performed, for example, by a library of submodule structures which are indexed according to FA tools.

The IC function modules are then mapped out on an IC design template (block 730) and unused areas of semiconductor material are identified. The analysis module, comprising the submodule test structures, is then mapped out on the IC design template (block 740), in these unused areas. The IC is then fabricated (block 750).

The testing and failure analysis of the IC is performed in two stages. In a first stage (block 760) the submodule test structures are analysed, in order to derive

performance parameters. These are then used in a second stage (block 770) to test the function modules of the IC. This then ends the process (block 780).

It will be appreciated that various general layout considerations will be taken into account when designing and fabricating the IC.

The analysis module can be operated using as fewer as 3 bumps that will be dedicated for the special test structures: Designated Vcc (fa_vcc), and GND (fa_gnd), that would enable an independent supply source to the test structures, and an input signal. These bumps will be biased or toggled accordingly.

Furthermore the substrates of some of the test structures will be connected to the chip default GND (fa_chip_gnd) and VCC (chip_vcc) in order to allow substrate current monitoring. The GND will be connected by default. However the connection of chip Vcc is selectively performed by Focus Ion Beam (FIB) modification from the front side of the die.

All of the submodule test structure functionality may be initiated by last metal connections or cuts (i.e. front side FIB modifications or with fuses).

By default the ring oscillator is disabled and the IREM cells (FIGS. 8-10) are disabled when the TRLEM cells are tested and vice versa. This conditioning is done by gating fa_gnd and fa_in, when fa_gnd=1 IREM1 cells are disabled and when fa_gnd=0 TRLEM cells are disabled.

Last metal modifications will be carried out either by disconnecting a supply to a certain line or by connection between two adjacent metal 5 lines. It is necessary to keep a minimum distance between two lines with the intention of future connection. Lines that are intended to be disconnected should be as narrow as possible.

As described above, the submodule test structures may include probing arrangements (such as the TRLEM probe chain) and optical alignment arrangements used for checking system integrity and for CAD alignment.

Also by default the drain, source and gate electrodes of all submodule test structure transistors will be connected to ground. With FIB all Vcc's and GND's will be connected to the designated supplies and each of the transistors gated could be separately connected to the fa_in signal. The substrates of the P or N transistors will be connected to the regular Vcc or GND respectively.

It will be understood that the analysis module, integrated circuit, system and method for testing an integrated circuit described above provides the following advantages:

With the complexity of design (over 50Mtransistors) and manufacturing process (<0.13um, >5 metal layers and above all flip-chip) failure analysis is a critical step in the process development. With the present invention it is possible to readily isolate desired parameters for calibration and testing. In this way the boundaries of

the specific process under examination may be determined at an early stage in the FA procedure, resulting in a significant time reduction without increasing the die size and without incurring any significant further cost.

It will be appreciated by a person skilled in the art that alternate embodiments to that described above are possible. For example, the present innovation is not limited to VLSI designs and may be incorporated into any new process design.

Furthermore the FA tools used for testing, and the number of FA tools used for any one IC may differ from those described above. Similarly the arrangements and number of associated submodule test structures may differ from those described above.

Claims

1. An analysis module for incorporation in an integrated circuit, the integrated circuit having circuit function modules, the analysis module including at least one submodule test structure arranged such that analysis of the at least one submodule test structure provides at least one physical parameter of the integrated circuit for use in subsequent testing of the circuit function modules.

2. An integrated circuit comprising:
circuit function modules arranged to provide operating functions of the integrated circuit; and,
an analysis module including at least one submodule test structure arranged such that analysis of the at least one submodule test structure provides at least one physical parameter of the integrated circuit for use in subsequent testing of the circuit function modules.

3. A system for testing integrated circuit functionality, the system comprising:
at least one analysis tool;
an integrated circuit having circuit function modules arranged to provide operating functions of the integrated circuit, and an analysis module including at least one submodule test structure,
wherein the at least one submodule test structure is arranged such that analysis of the at least one submodule test structure by the at least one analysis tool provides at least one physical parameter of the integrated circuit

for use in subsequent testing of the circuit function modules by the at least one analysis tool.

4. The analysis module, integrated circuit or system of any preceding claim wherein the at least one submodule test structure is chosen in dependence upon the at least one analysis tool to be used in subsequent testing.

5. A method for testing integrated circuit functionality, the method comprising:
selecting at least one analysis tool to be used for testing an integrated circuit;
selecting at least one submodule test structure in dependence upon the chosen at least one analysis tool;
designing circuit function modules of the integrated circuit arranged to provide operating functions of the integrated circuit;
designing an analysis module of the integrated circuit including the at least one submodule test structure,
fabricating the integrated circuit;
analysing the at least one submodule test structure by the at least one analysis tool in order to provide at least one physical parameter of the integrated circuit; and,
testing of the circuit function modules by the at least one analysis tool using the at least one physical parameter.

6. The analysis module, integrated circuit, system or method of any preceding claim wherein the at least one

submodule test structure includes a calibration structure.

7. The analysis module, integrated circuit, system or method of any preceding claim wherein the at least one submodule test structure includes a probing structure.

8. The analysis module, integrated circuit, system or method of any preceding claim wherein the at least one submodule test structure includes optical alignment means.

9. The analysis module, integrated circuit, system or method of any preceding claim wherein the at least one submodule test structure is isolated from the function modules.

10. The analysis module, integrated circuit, system or method of any preceding claim wherein the testing includes failure analysis, system calibration and evaluation.

11. An analysis module substantially as hereinbefore described with reference to the accompanying drawings.

12. An integrated circuit substantially as hereinbefore described with reference to the accompanying drawings.

13. A system substantially as hereinbefore described with reference to the accompanying drawings.

14. A method for testing integrated circuit functionality substantially as hereinbefore described with reference to the accompanying drawings

Abstract

ANALYSIS MODULE, INTEGRATED CIRCUIT, SYSTEM AND METHOD FOR TESTING AN INTEGRATED CIRCUIT

(with reference to FIG. 1)

A system (5) for testing and failure analysis of an integrated circuit (10) is provided using failure analysis tools (40, 50, 60). An analysis module (30) having a number of submodule test structures is incorporated into the integrated circuit design. The test structures are chosen in dependence upon the failure analysis tools (40, 50, 60) to be used. The rest of the integrated circuit contains function modules (20) arranged to provide normal operating functions. By analysing the submodule test structures of the analysis module (30) using the failure analysis tools(40, 50, 60), physical parameters of the integrated circuit (10) are obtained and used in subsequent testing of the function modules (20) by the failure analysis tools(40, 50, 60), thus simplifying the testing of the integrated circuit (10) and reducing the time taken to perform a failure analysis procedure.

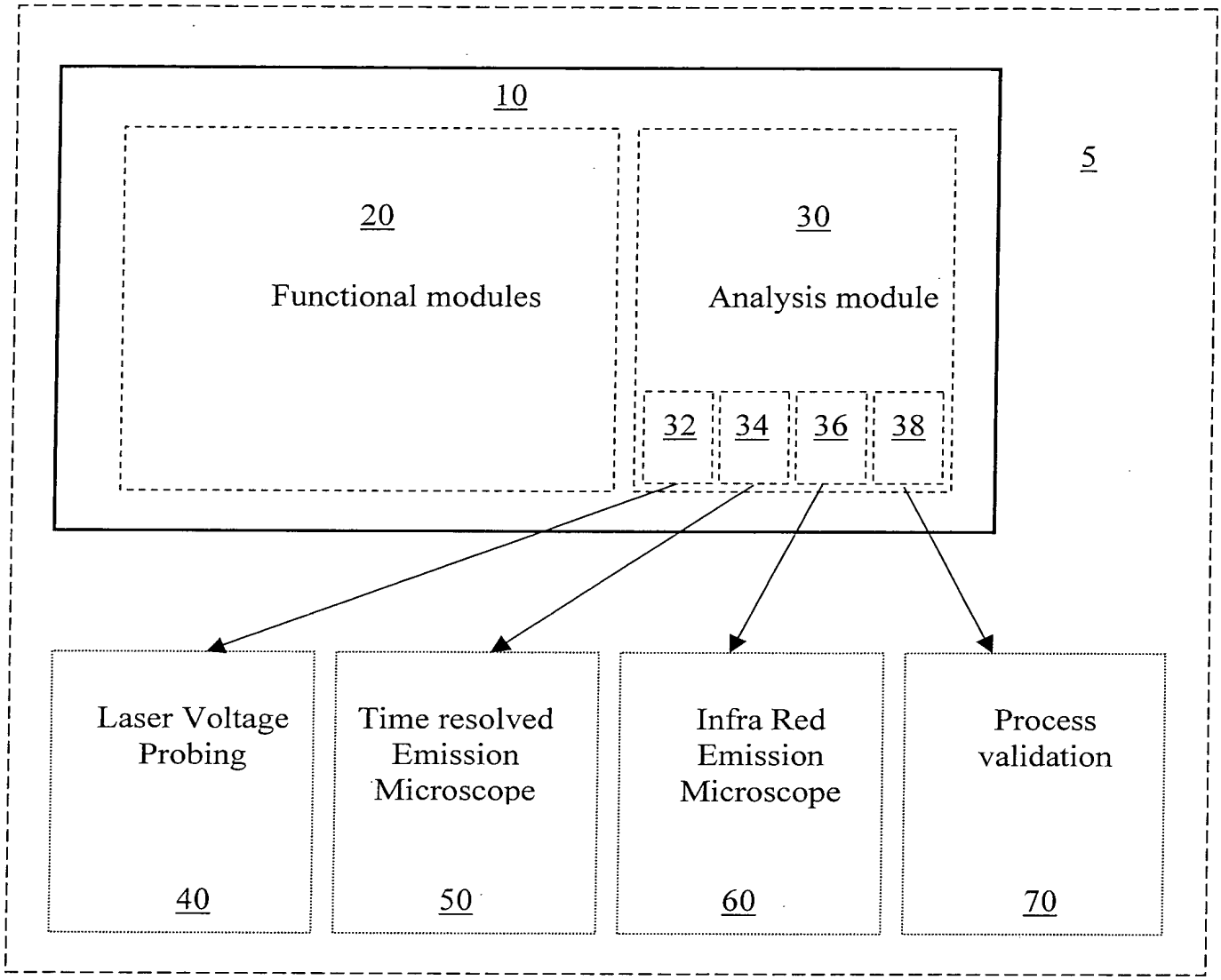
10
5
20
Functional modules
30
Analysis module
32
34
36
38
Laser Voltage Probing
40
Time resolved Emission Microscope
50
Infra Red Emission Microscope
60
Process validation
70

FIG. 1

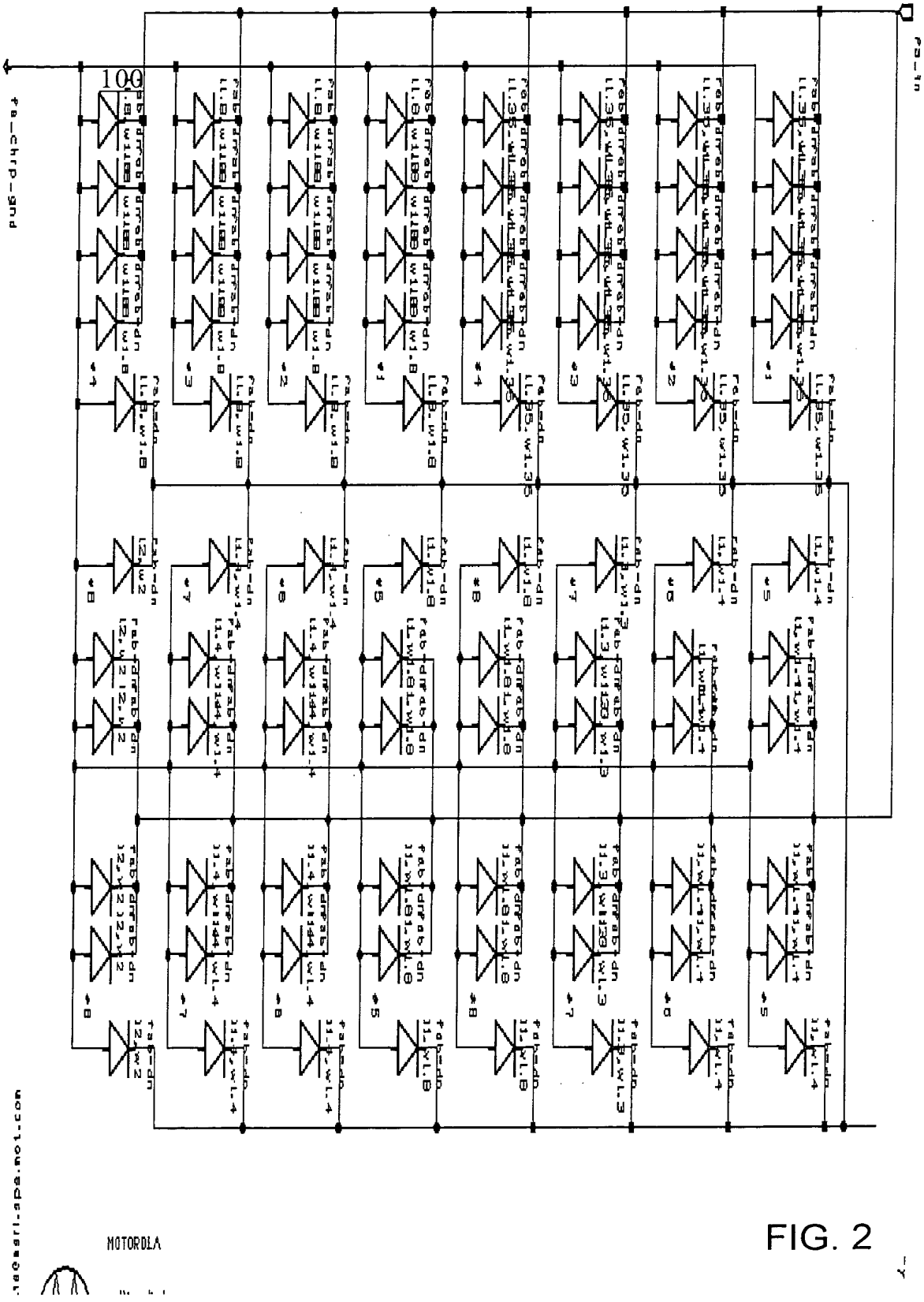

FIG. 2

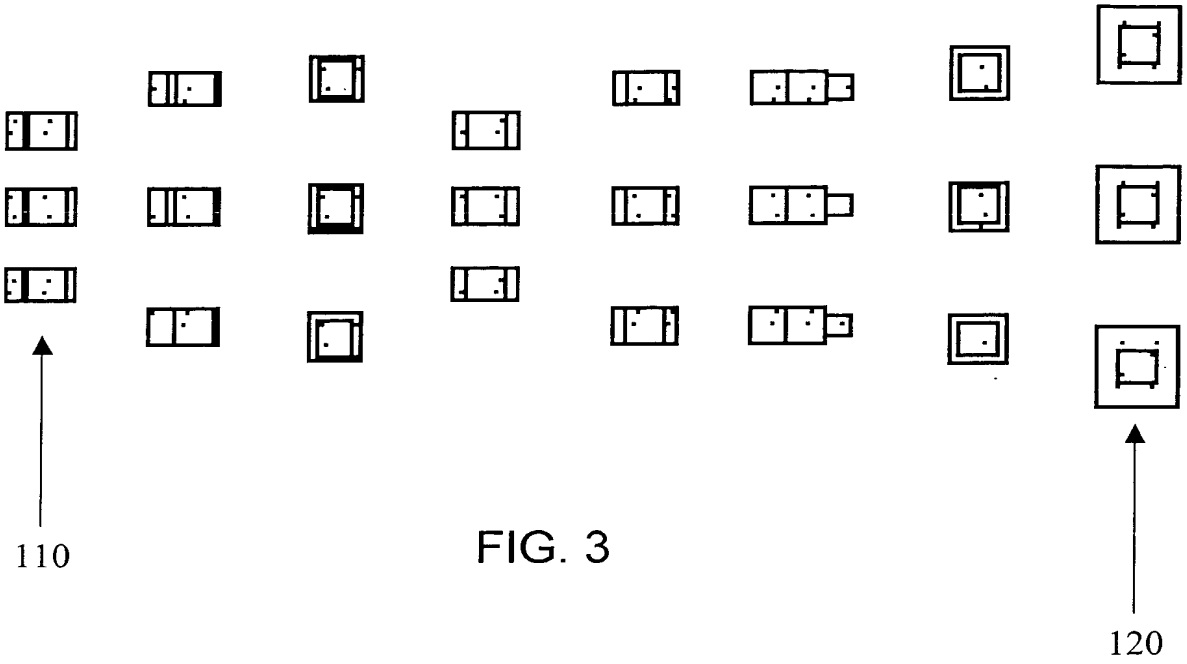

FIG. 3

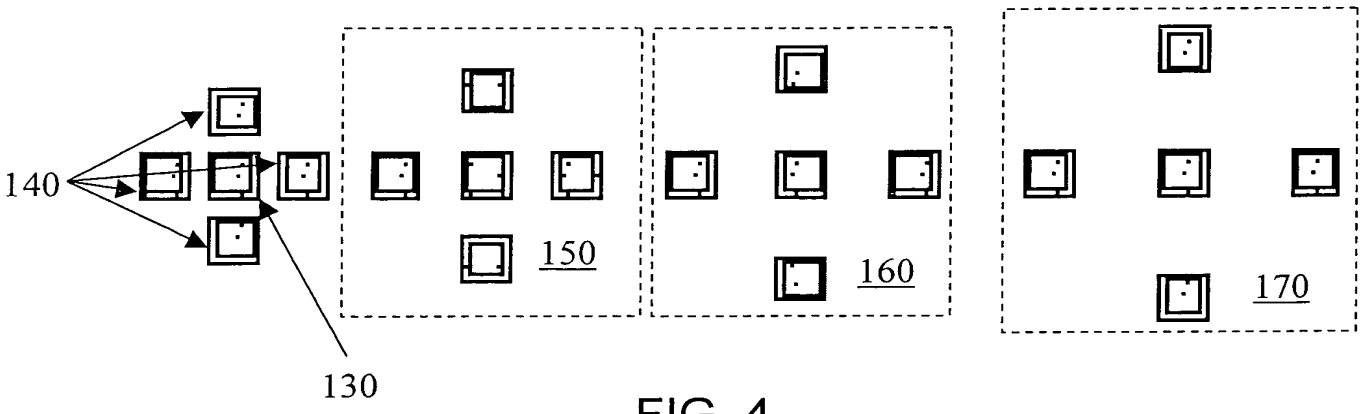

FIG. 4

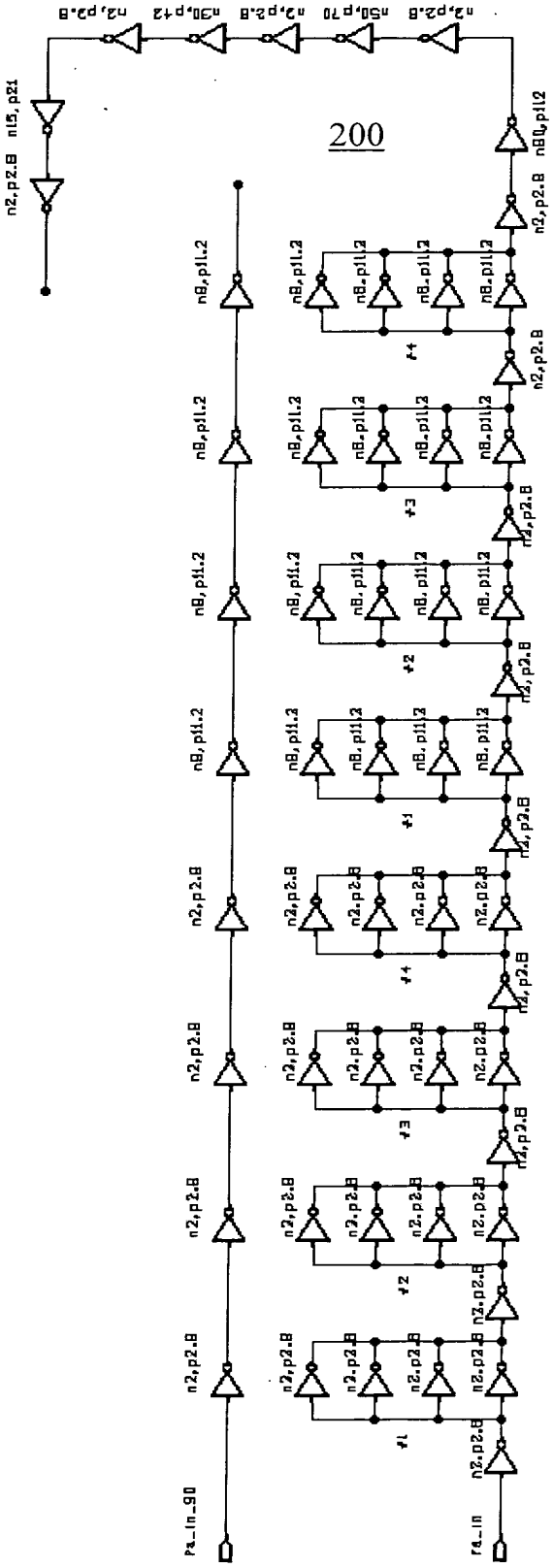

FIG. 5

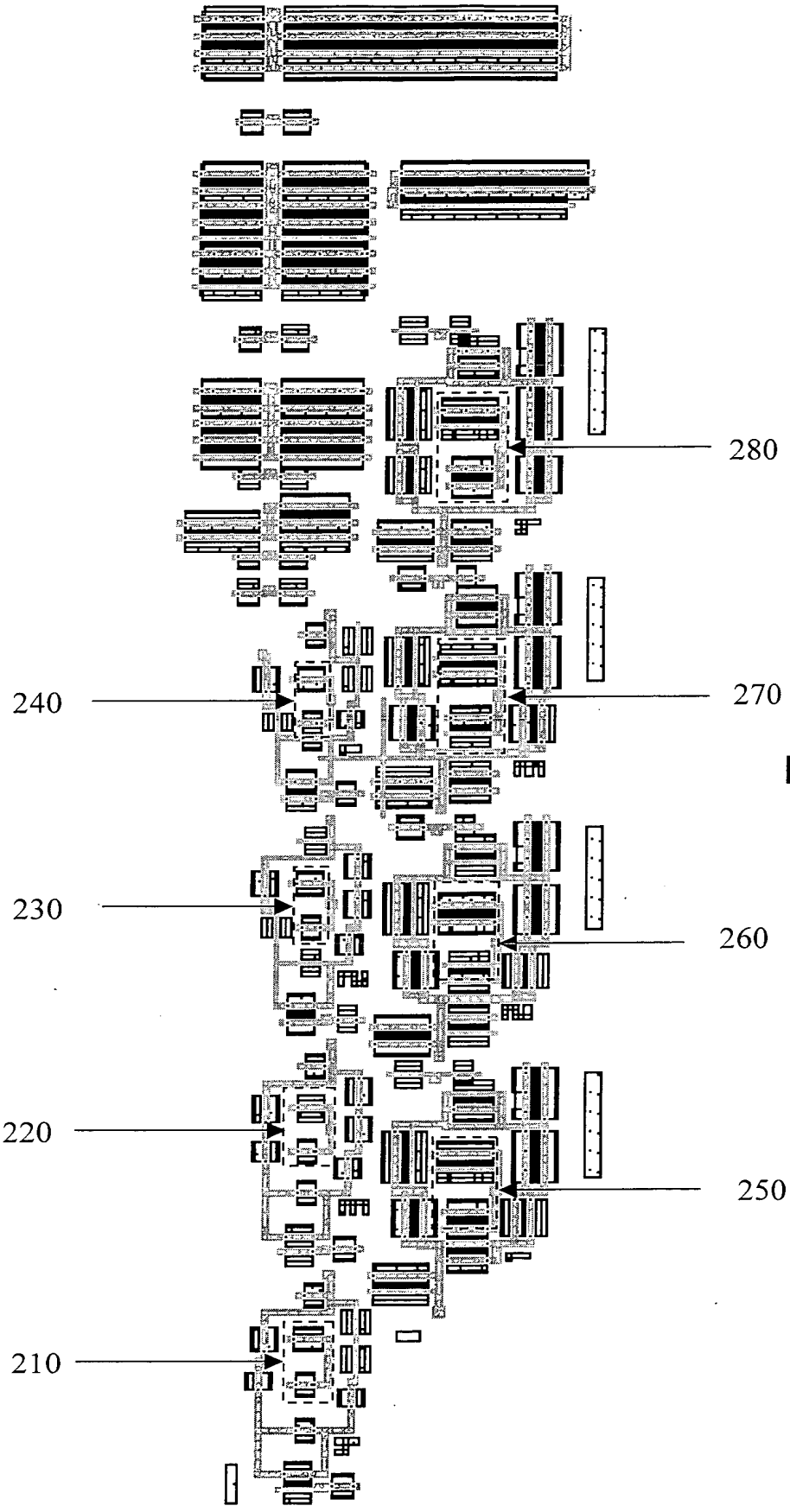

FIG. 6

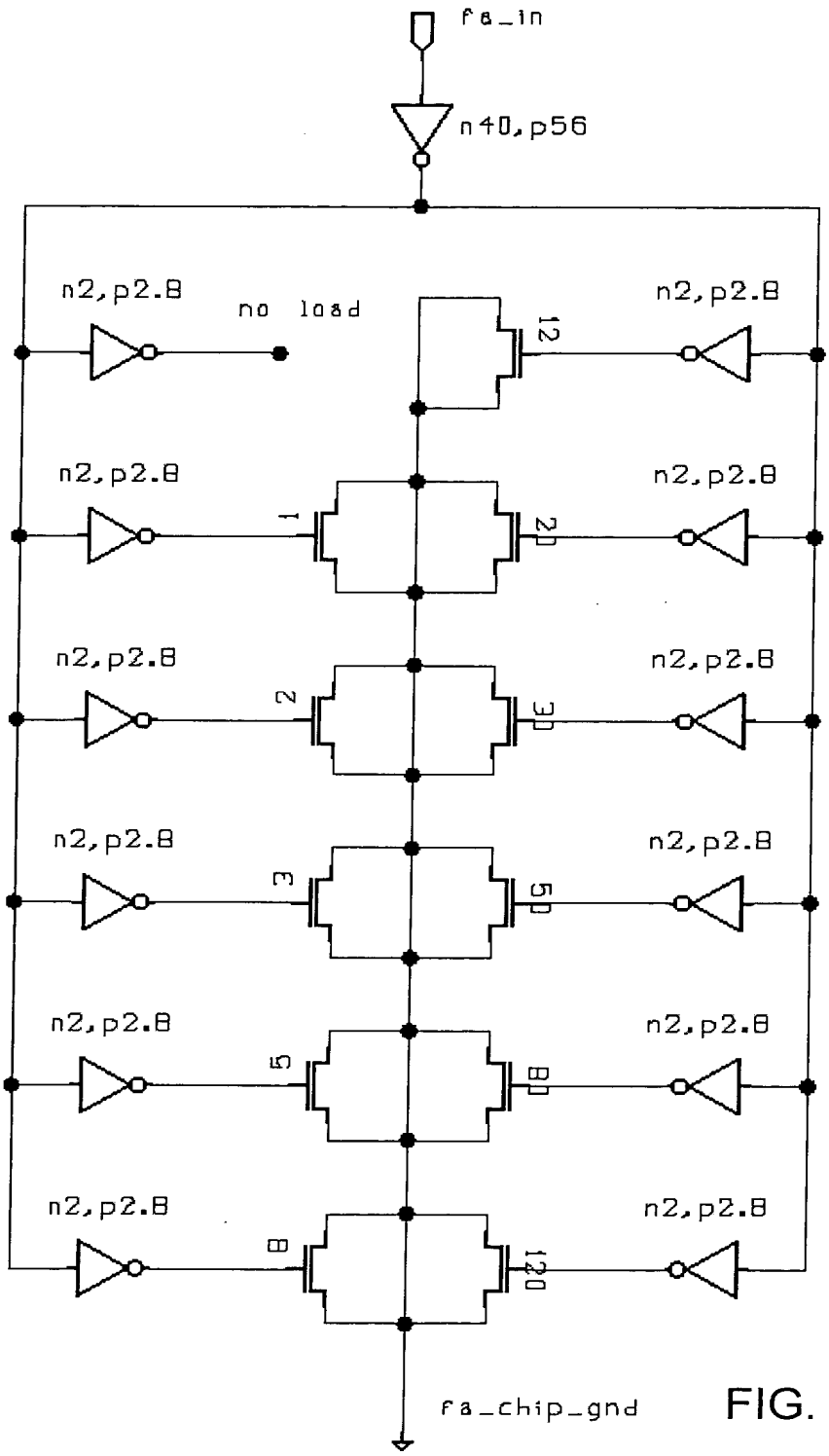
fa_in
n40,p56
n2,p2.8
no load
n2,p2.8
12
n2,p2.8
n2,p2.8
1
20
n2,p2.8
n2,p2.8
2
30
n2,p2.8
n2,p2.8
3
50
n2,p2.8
n2,p2.8
5
80
n2,p2.8
n2,p2.8
8
120
n2,p2.8
fa_chip_gnd

FIG. 7

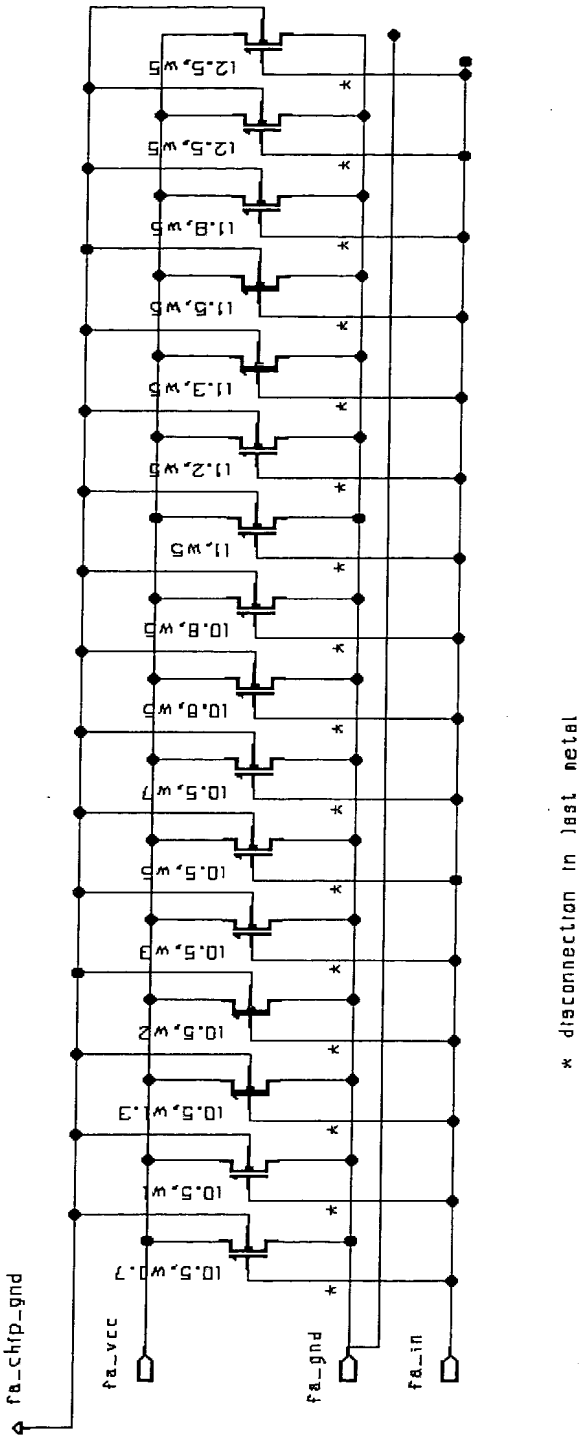
fa_chip_gnd
fa_vcc
fa_gnd
fa_in
10.5,w0.7
10.5,w1
10.5,w1.3
10.5,w2
10.5,w3
10.5,w5
10.5,w7
10.8,w5
10.8,w5
11,w5
11.2,w5
11.3,w5
11.5,w5
11.8,w5
12.5,w5
12.5,w5
* disconnection in last metal

FIG. 8

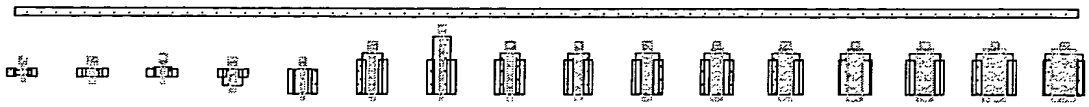

FIG. 9

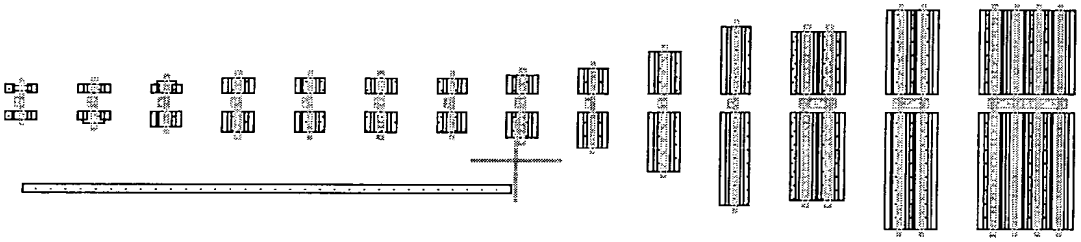

FIG. 10

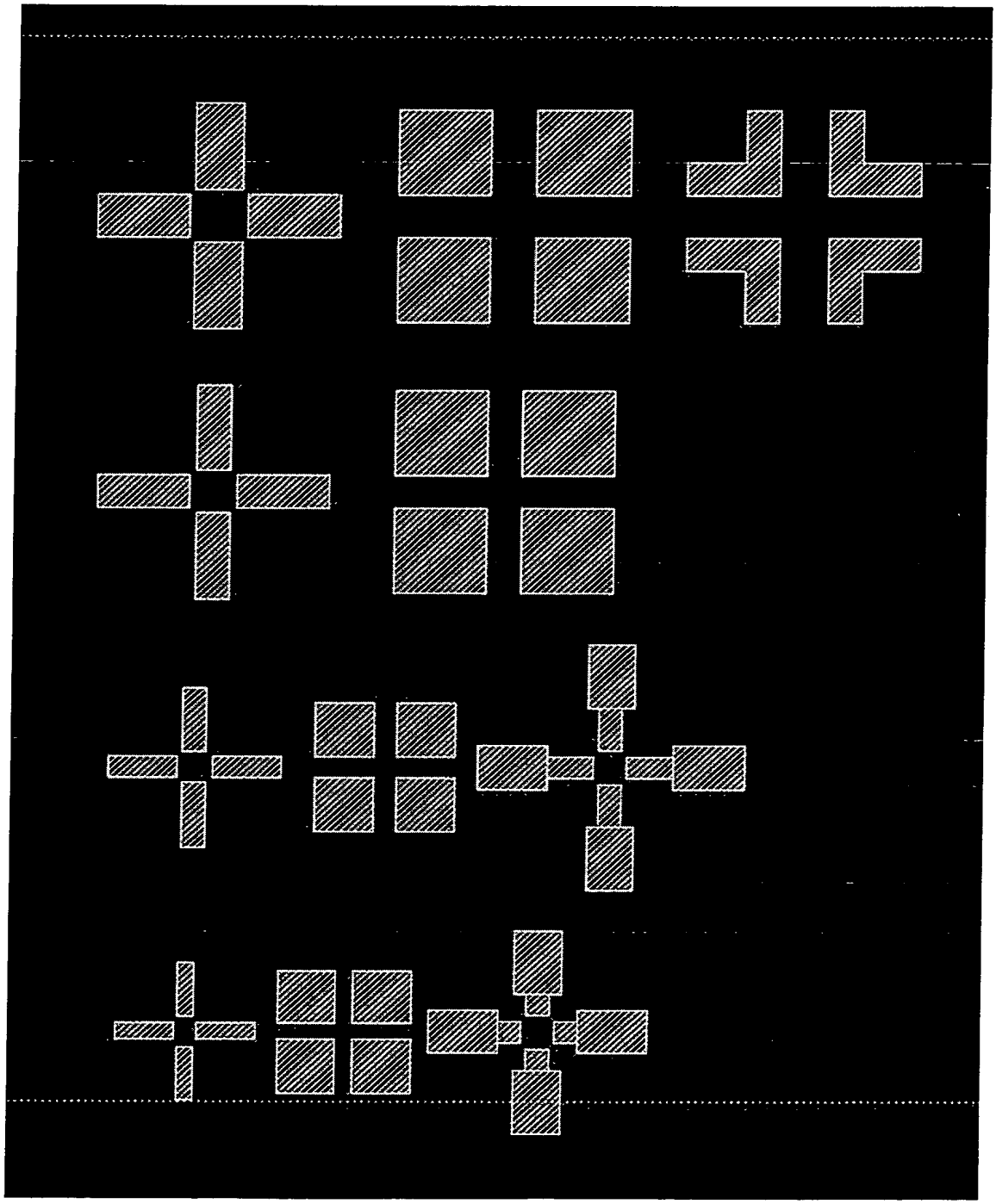

FIG. 11

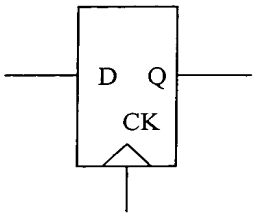

FIG. 12

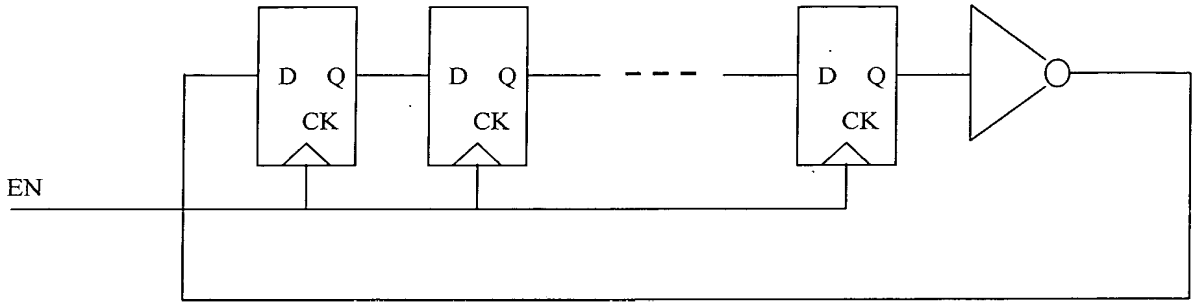

FIG. 13

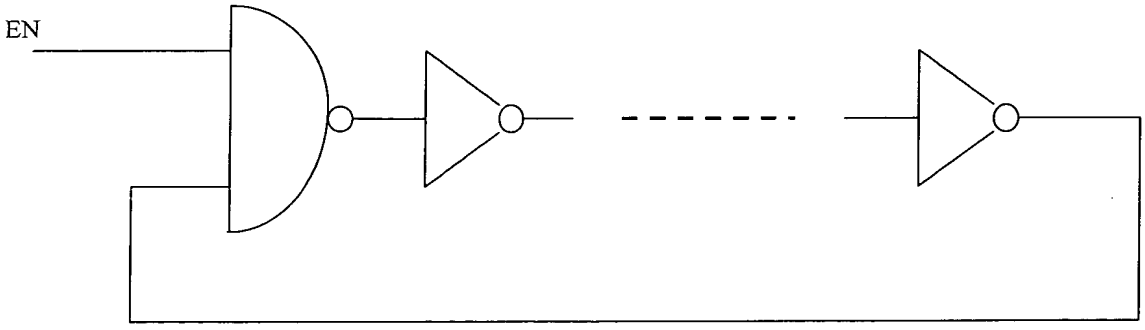

FIG. 14

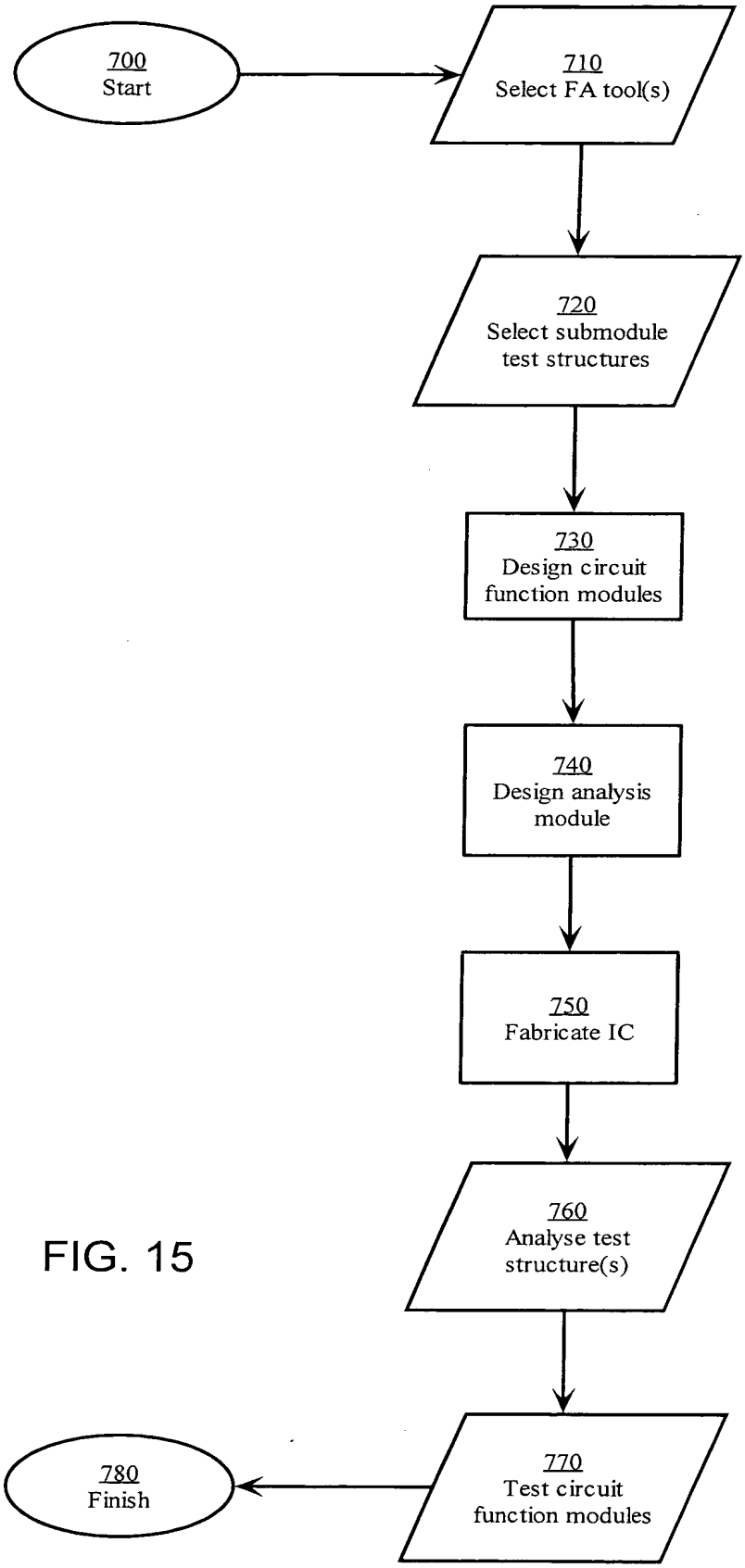
700
Start
710
Select FA tool(s)
720
Select submodule test structures
730
Design circuit function modules
740
Design analysis module
750
Fabricate IC
760
Analyse test structure(s)
770
Test circuit function modules
780
Finish

FIG. 15